Claims

The following is a copy of Applicants' claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~——~~"), as is applicable:

1. (Currently Amended) A method for generating a random bit stream comprising:

accumulating a plurality of hardware driven numbers;

extracting a portion of each hardware driven number, the portion less than the whole of each hardware driven number; and

combining each extracted portion to form a random bit stream.

2. (Currently Amended) The method of claim 1 wherein accumulating ~~a~~the plurality of hardware driven numbers comprises:

reading a timestamp; and

storing the timestamp.

3. (Currently Amended) The method of claim 2 wherein extracting ~~a~~the portion of each hardware driven number comprises extracting one or more lower order bits from each hardware driven number.

4. (Currently Amended) The method of claim 1 wherein accumulating ~~a~~the plurality of hardware driven numbers comprises:

determining ~~the~~a quantity of the plurality of hardware driven numbers required to achieve a pre-established output bit rate using a predefined de-skewing mechanism; and

accumulating the determined quantity of the plurality of hardware driven numbers.

5. (Currently Amended) The method of claim 1 wherein extracting ~~a~~the portion of each hardware driven number comprises extracting one or more bits from each hardware driven number.

6. (Currently Amended) The method of claim 1 wherein combining each extracted portion comprises:

concatenating bits extracted from each hardware driven number at a particular bit position; and

de-skewing ~~the~~a concatenated result in order to provide a uniform distribution of random bits.

7. (Currently Amended) An apparatus for generating a random bit stream comprising:

a number receiver that receives hardware driven numbers;

an extractor that extracts a portion of a hardware driven number, the portion less than the whole of the hardware driven number; and

a bit stream generator that generates a bit stream according to a plurality of extracted portions of the hardware driven numbers.

8. (Currently Amended) The apparatus of claim 7 wherein the number receiver comprises:

a time interface that ~~is capable of receiving~~receives a timestamp; and

a buffer that stores the timestamp.

9. (Currently Amended) The apparatus of claim 8 wherein the extractor comprises a selection matrix that selects one or more ~~of the~~ least significant bits in the timestamp.

10. (Currently Amended) The apparatus of claim 7 further ~~comprises~~ comprising a cycle generator that comprises:

a time base generator that generates a time base;

a translation table that generates a de-skewing factor according to a bit rate indicator; and

a count down divider that generates a number pulse by dividing the time base according to the de-skewing factor and wherein the translation table is populated with empirical data that correlates ~~the~~ an efficiency of a de-skewing mechanism associated with the de-skewing factor and the bit rate indicator.

11. (Currently Amended) The apparatus of claim 7 wherein the extractor comprises:

one or more input ports, each for receiving a data bit;

one or more output ports, each for driving a data bit; and

cross-bar switch for connecting ~~a~~the data bit from ~~an~~the one or more input ~~port~~ports to at least one of the output ~~port~~ports.

12. (Currently Amended) The apparatus of claim 7 wherein the bit stream generator comprises:

a plurality of registers that accept extracted portions of the hardware driven numbers and present a bit-wise concatenated result;

a transition mapping table populated with de-skewing values that generates a de-skewed random number according to the concatenated result; and

a shift register that serializes the de-skewed random number.

13. (Currently Amended) A random bit stream generator comprising:

a processor ~~capable of executing~~ configured to execute instructions;

a memory; and

instruction sequences stored in the memory comprising:

a number receiver module that, when executed by the processor, minimally causes the processor to retrieve a hardware driven number;

an extractor module that, when executed by the processor, minimally causes the processor to extract a portion of ~~a~~the hardware driven number; and

a concatenator module that, when executed by the processor, minimally causes the processor to generate a concatenated value by combining a plurality of extracted portions of hardware driven numbers in a bit-wise manner.

14. (Currently Amended) The random bit stream generator of claim 13 further comprising a serializing output register ~~capable of generating~~ that generates a serial bit stream according to at least one of the concatenated value and a de-skewed concatenated value.

15. (Currently Amended) The random bit stream generator of claim 13 further comprising a hardware number generator ~~capable of generating~~ that generates a timestamp and wherein the number receiver module minimally causes the processor to:

retrieve ~~a~~the timestamp from the hardware number generator; and

store the timestamp in a buffer region in the memory.

16. (Currently Amended) The random bit stream generator of claim 15 wherein the extractor module minimally causes the processor to extract ~~a~~the portion of ~~a~~the hardware driven number by extracting one or more lower order bits from ~~a~~the hardware driven number.

17. (Currently Amended) The random bit stream generator of claim 13 further comprising a number pulse generator that ~~is capable of issuing~~issues a number pulse signal to the processor and wherein the number receiver module minimally causes the processor to retrieve ~~a~~ the hardware number from ~~a~~the hardware number generator according to the number pulse signal and wherein ~~the~~a period of the number pulse signal is selected according to a pre-established output bit rate using a predefined de-skewing mechanism.

18. (Currently Amended) The random bit stream generator of claim 13 wherein the extractor module minimally causes the processor to extract ~~a~~the portion of ~~a~~the hardware driven number by minimally causing the processor to extract one or more bits from the hardware driven number.

19. (Original) The random bit stream generator of claim 13 further comprising a de-skewing module instruction sequence stored in the memory that, when executed by the processor, minimally causes the processor to de-skew the concatenated value.

20. (Currently Amended) A computer-readable medium having stored therein computer-executable functions for generating a random bit stream, comprising:

a number receiver instruction sequence that, when executed by a processor, minimally causes the processor to accumulate a plurality of hardware driven numbers;

an extractor instruction sequence that, when executed by ~~a~~the processor, minimally causes the processor to extract a portion of each hardware driven number; and

a concatenator instruction sequence that, when executed by ~~a~~the processor, minimally causes the processor to concatenate a plurality of extracted portions of the hardware driven numbers into a concatenated value in a bit-wise manner.

21. (Currently Amended) The computer-readable medium of claim 20 wherein the number receiver instruction sequence minimally causes the processor to accumulate ~~a~~the plurality of hardware driven numbers by minimally causing the processor to:

read a timestamp from a hardware driven number generator; and

store the timestamp in a memory.

22. (Currently Amended) The computer-readable medium of claim 21 wherein the extractor instruction sequence minimally causes the processor to extract ~~a~~the portion of each hardware driven number by minimally causing the processor to extract one or more lower order bits from the timestamp.

23. (Currently Amended) The computer-readable medium of claim 20 wherein the number receiver instruction sequence minimally causes the processor to accumulate ~~a~~the plurality of hardware driven numbers by minimally causing the processor to accumulate a quantity of the hardware driven numbers over a period of time, wherein the quantity of hardware driven numbers ~~accumulate~~ accumulated over the period of time is selected according to a pre-established output bit rate and a predefined de-skewing mechanism.

24. (Currently Amended) The computer-readable medium of claim 20 wherein the extractor instruction sequence minimally causes the processor to extract ~~a~~the portion of each hardware driven number by minimally causing the processor to extract one or more bits from each hardware driven number.

25. (Currently Amended) The computer-readable medium of claim 20 further comprising a de-skewing instruction sequence that, when executed by ~~a~~the processor, minimally causes the processor to de-skew the concatenated value.

26. (Original) A random bit stream generator comprising:

means for accumulating a plurality of hardware driven numbers;

means for extracting a portion of each hardware driven number; and

means for combining each extracted portion to form a random bit stream.

27. (Original) The random bit stream generator of claim 26 wherein the accumulating means comprises:

means for reading a timestamp; and

means for storing the timestamp.

28. (Currently Amended) The random bit stream generator of claim 26 wherein the accumulating means comprises:

means for accumulating a selected quantity of the hardware driven numbers over a period of time, wherein the selected quantity is selected according to a pre-established output bit rate and a predefined de-skewing mechanism.

29. (Original) The random bit stream generator of claim 26 wherein the extracting means comprises a means for extracting one or more bits from a hardware driven number.

30. (Original) The random bit stream generator of claim 26 wherein the combining means comprises:

concatenating means for bit-wise concatenating the extracted portions into a concatenated value; and

de-skewing means for de-skewing the concatenated value in order to result in a uniform distribution of random bits.